12 Switch Zero-Inductor Voltage Converter Topology

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***Abstract*—The demand for internet and computing resources has led to datacenters and servers being one of the fastest growing consumers of power in the world today. While datacenter power architectures have improved over time, the majority of the loss still occurs at the server power supply, and board level voltage regulators. To attempt to improve this, Google has proposed and implemented a 48 volt server architecture that can significantly reduce both the upstream conversion losses, and the distribution losses within the server racks. Google has estimated that this change can reduce their overall conversion losses by up to 30%, but to fully realize these benefits new technology is needed to convert 48 volts down to the point of load voltage levels. The Intermediate Bus Architecture, where a "bus converter" steps down the 48 volts to a lower bus voltage which is then stepped down by point-of-load regulators is a very attractive option to "bridge the gap" between the 48 volt architecture of cutting edge servers, and the existing 12 volt architecture. The proposed topology is a novel intermediate bus converter that can achieve up to 990W/in^3 power density, 99.2% peak efficiency, and 97.8% full load efficiency for 65A 12V output. Compared with other cutting edge designs this work achieves higher efficiency, and superior power density without the need for complex control, or a sensitive resonant based design.**

Keywords—DC-DC Converter, Datacenter, Intermediate Bus

I. Introduction

Datacenters and servers are one of the largest growing consumers of electrical power in the world today. The Information and Communication Technology (ICT) sector consumes approximately 7% of the world's electricity today, and this number is projected to rise to 13% by 2030 [1]. With advances in cloud computing, and the massive expansion in the use of internet services worldwide, datacenters are expected to be one of the fastest growing consumers of electricity within the ICT sector, increasing by up to 20% per year. In 2017 there are 8.4 billion "internet of things" connected devices. This is expected to rise to over 20 billion devices by 2020, as over 1 billion new internet users are expected to emerge during that time, growing from 3 billion to over 4 billion.

Datacenter architecture has evolved over time, and significant gains have been realized at the building level power conversion steps, however, the majority of the loss still occurs at the server PSU and board-level voltage regulators. Google's approach has been to implement what they refer to as a 48 volt power architecture [4]. In this architecture the server PSU distributes 48 volts throughout the server rack, which is then converted to the voltage required at the point of load. Google has estimated that this change can reduce their conversion losses 30%, as well as offering a 16x reduction in the distribution losses throughout the rack [5]. Overall this has the potential to greatly reduce cost and improve both efficiency and flexibility. However, this 48 volt to POL conversion can be very challenging, particularly for low voltage high current loads such as modern processors. The most common approach is to utilize a "two-stage" conversion approach, such as the Intermediate Bus Architecture, to achieve this stepdown at high efficiency [6][7]. The topology proposed in this paper is a novel topology for an intermediate bus converter based on the Zero-Inductor Voltage (ZIV) Converter aimed at 48 volt datacenter applications [8].

Table 1 Efficiency Breakdown of Server Power Supplies [2][3]

UPS	PDU	Rack-Level Converter	**Server PSU**	**VR Stage**	Overall
Traditional AC					
89.2	93.2	N/A	**75.5**	**81.6**	51.6
High-Efficiency AC					
97.1	94.0	N/A	**88.0**	**87.7**	69.9
Rack-Level 48VDC					
97.1	93.8	92.38	**91.5**	**87.7**	67.4
Facility-Level 400VDC					
95.3	96.8	N/A	**89.1**	**87.7**	72.7

II. Topology Overview

A. Operating Principles

The single-phase 7-switch ZIV Converter, along with the PWM signal diagram is shown in Figures 1 and 2. In this topology the first-stage switches (M1-M4) operate with only 25% duty cycle. This causes relatively large RMS current stress through the MOSFETs, input capacitor, and first-stage flying capacitor. In order to improve the efficiency, the 12-switch ZIV converter proposed in this paper is shown in Figure 3. This converter utilizes two paralleled second-stages, but requires only a single input-stage. This results in significant component and size savings compared with a "true" two-phase ZIV converter, while also offering greatly improved efficiency when compared with a single-phase ZIV converter. The operation of this topology, and the realization of the component reduction, is best understood by examining two single-phase ZIV converters operating in parallel with a 180 degree phase shift. Note that for each phase, the first stage switches M1-M4 will be off for 50% of the total converter cycle during State C, as shown in Figure 2.

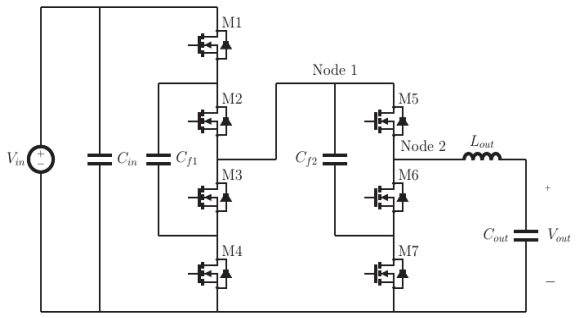

Fig. 1. Single-Phase ZIV Converter

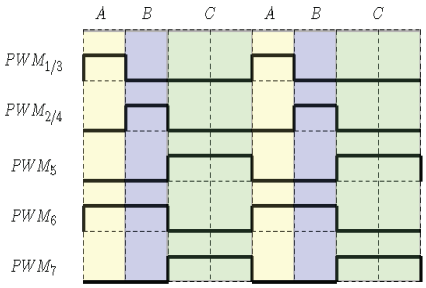

Fig. 2. Single-Phase ZIV Converter Gate Drive Diagram

Instead of having two first-stages, each operating for only 50% of the total cycle, it is possible to drive a single first stage at double the frequency. When one of the phases enters State C, the additional MOSFETs M5 or Q5 will block the voltage at Node 1 from being pulled down to the output voltage. This allows the two input stages to be consolidated into a single stage, producing the PWM gate diagram in Figure 4. This component count reduction can be achieved without a significant loss penalty; considering the first-stage MOSFET's of a single-phase ZIV converter the total RMS current stress for each MOSFET will be given by:

$$I_{RMS(M1-M4)} = \sqrt{0.25} I_{out} = \frac{I_{out}}{2} \quad (1)$$

For the flying capacitor the RMS current stress will be given by:

$$I_{RMS(C_{f1})} = \sqrt{0.5} I_{out} = \frac{\sqrt{2}}{2} I_{out} \quad (2)$$

In the twelve-switch ZIV Converter:

$$I_{RMS(M1-M4)} = \frac{\sqrt{0.5} I_{out}}{2} = \frac{\sqrt{2}}{4} I_{out} \quad (3)$$

For the flying capacitor:

$$I_{RMS(C_{f1})} = \frac{I_{out}}{2} \quad (4)$$

So, compared with a single phase ZIV converter, the total conduction loss in the first stage will be reduced by a factor of 2. This offers a significant performance improvement over a single phase ZIV converter, without requiring a doubling of the component count such as in a true two-phase ZIV converter. The switching loss for MOSFETs M1-M4 in the 12 switch converter will be the same as a single phase ZIV converter for the same output load. This is because while the switching frequency is doubled, the current at the time of switching will be halved. The increased switching frequency reduces the flying capacitor ripple in the first stage and the 50% duty cycle operation also reduces the input capacitor RMS current compared with a single-phase ZIV converter. In the single-phase ZIV converter the input capacitor RMS is given by:

$$I_{RMS(C_{in})} = \sqrt{\left(\frac{3}{4} I_{out} \sqrt{0.25}\right)^2 + \left(\frac{1}{4} I_{out} \sqrt{0.75}\right)^2} = \frac{\sqrt{3}}{4} I_{out} \quad (5)$$

For the 12 switch topology M1 now operates at 50% duty cycle, and therefore charges and discharges at 1/4 of the output current, reducing the input capacitor losses by a factor of 3:

$$I_{RMS(C_{in})} = \frac{1}{4} I_{out} \quad (6)$$

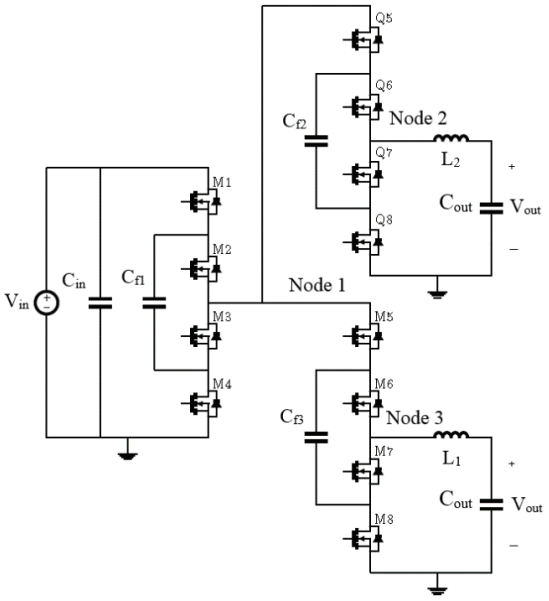

Fig. 3. 12-Switch ZIV Converter

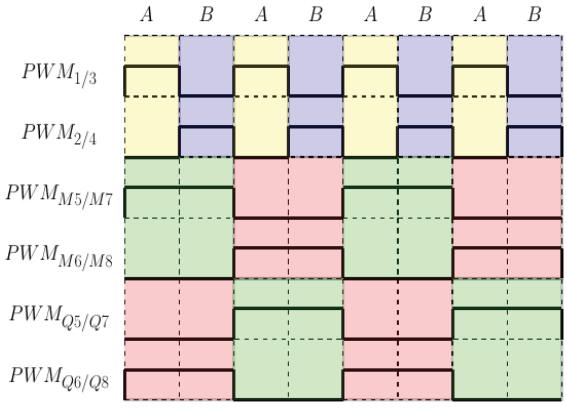

Fig. 4. 12-Switch ZIV Converter Gate Diagram

B. Capacitor Balancing and Start-Up

Active capacitor balancing is not required for the proposed topology. This can be explained by examining the circuit in Figure 5. This circuit represents one of the four switch "building-blocks" that make up the converter. If we neglect the capacitor ripple then the steady state voltage for the capacitor can be found as follows. Let D be the duty cycle for the pair of switches M1 and M3, and let 1-D be the duty cycle for the pair of switches M2 and M4.

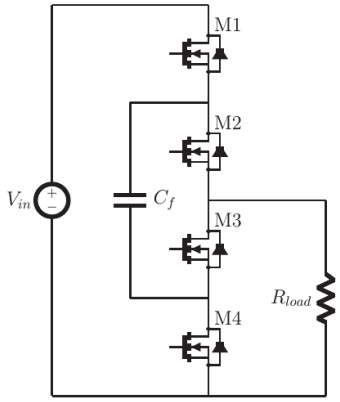

Fig. 5. Switched Capacitor "Building-Block"

$$I_1 = \frac{V_{in} - V_{cap}}{R} \tag{6}$$

$$I_2 = \frac{-V_{cap}}{R} \tag{7}$$

Then by noting that for steady state the average current through the capacitor for one switching cycle must be zero:

$$I_{avg} = I_1(D) + I_2(1-D) = 0 \tag{8}$$

$$D(V_{in} - V_{cap}) = (1-D)(V_{cap}) \tag{9}$$

$$V_{cap} = DV_{in} \tag{10}$$

What is important to note here is that the capacitor voltage does not "run-away" to V_{in} or zero, it is determined by the duty cycle. Therefore there is no need for active balancing as in practice any mismatch in duty cycles should be small and therefore the capacitor voltage will be very close to the expected value.

This result is also verified in the simulation results section III-B. It should be noted that without a pre-charge circuit the peak MOSFET voltage during start-up will be increased, and the charging current may cause unacceptable current spikes. Therefore, a soft-start pre-charging circuit such as in [9] is recommended unless the circuit can be started at a reduced input voltage. Active balancing of the capacitors is not required under start-up or steady-state operation.

III. Simulation Results

A. Key Operating Waveforms

In order to demonstrate the operation of the proposed topology simulation waveforms are presented. The simulation parameters are shown in Table 2. Note that the base frequency is given at 60kHz. This means M1-M4 are switched at twice the this frequency, or 120kHz.

Table 2 Simulation Parameters

Simulation Parameters	
Switching Frequency	60kHz
Input Voltage	48V
Load Current	30A
Deadtime	100nsec
Inductor Value	200nH
Capacitor Value	100uF

Figure 6 shows the input voltage, Node 1 voltage, and output voltage for the circuit. This demonstrates the 4:1 step-down achieved by the topology. Note that Node 1 is pulled down to the output voltage during the switching transition, however, M5 and Q5 block this during normal operation outside of the deadtime. Note that this deadtime pulse on Node 1 will change in value depending on whether one MOSFET or two MOSFETs are reverse conducting during the associated switching transition deadtime.

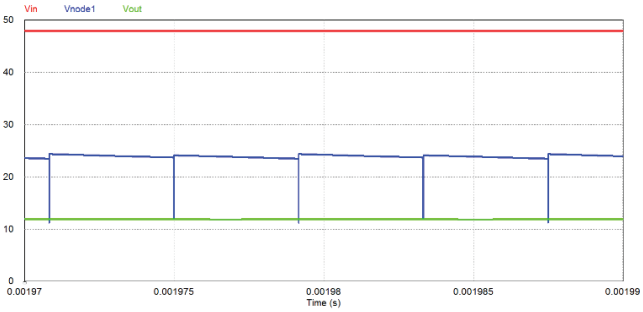

Fig. 6. Input Voltage, Node 1 Voltage, Output Voltage Waveforms

Figure 7 shows the capacitor voltage waveforms for Cf1 to Cf3. The output voltage of each phase, before filtering, at Node 2 and Node 3, as well as the filtered output voltage is presented in Figure 8. This Figure demonstrates the key advantage of the topology, namely the "zero-inductor voltage" is maintained in this 12-Switch topology. The negative pulses on the output voltage before filtering are due to the dead-time included in the simulation, and otherwise the voltage across the inductor is only capacitor ripple. Note that similar to Node 1 the magnitude of the negative pulses will change based on whether one or two MOSFETs are reverse conducting during the deadtime.

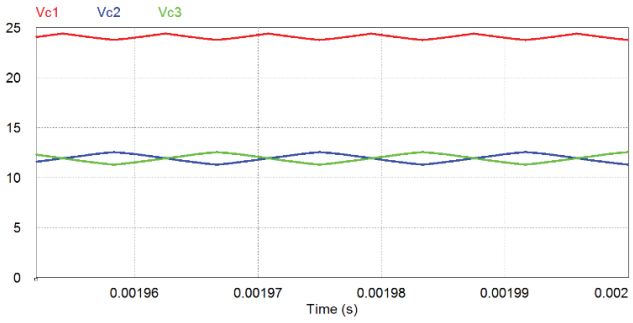

Fig. 7. C_{f1}, C_{f2} and C_{f3} Voltage Waveforms

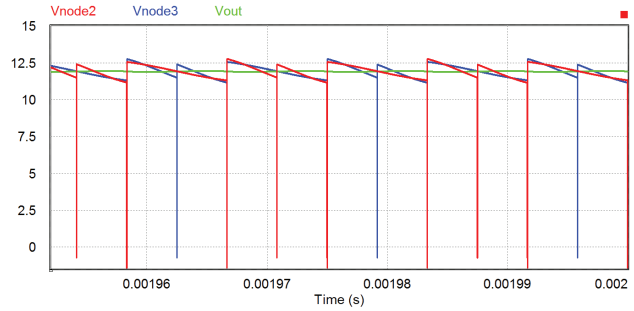

Fig. 8. Node 2, Node 3 and Output Voltage Waveforms

The current waveforms for M1 and M2 are shown in Figure 9. These waveforms demonstrate the key advantage of the 12-switch topology; namely that superior switch utilization can be achieved by operating the first stage at twice the frequency of the second stages. As shown, the duty cycle of the MOSFETs is raised from 25% in the single-phase ZIV topology to 50% in the 12-switch topology, and the MOSFET conducts only half of the total load current. This validates the analysis of the RMS current reduction presented in Section II-A. The inductor current waveforms are shown in Figure 10. This shows that the two output stages are operating at 180 degrees out of phase, and each phase carries one-half of the total load current. It is noted that the inductor current ripple is small despite using a 200nH inductor with only 60kHz switching frequency.

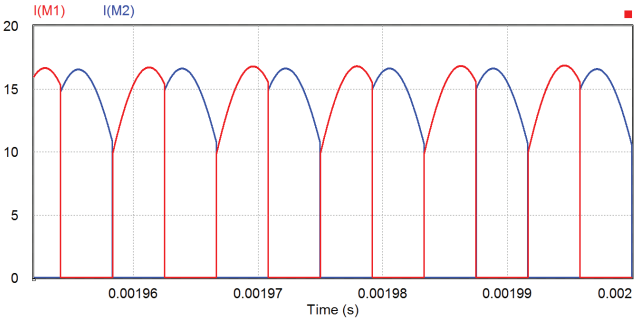

Fig. 9. M1 and M2 Current Waveforms

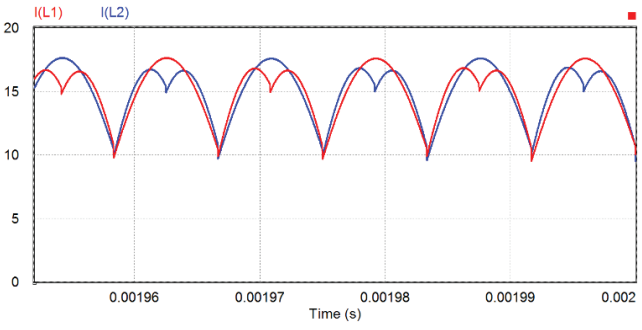

Fig. 10. Inductor Current Waveforms

B. Capacitor Balancing

The capacitor waveforms during start-up, with no soft-starting, are shown in Figure 11. This simulation verifies that, without any pre-charging, the capacitors settle at their expected steady-state values with no active balancing or control required.

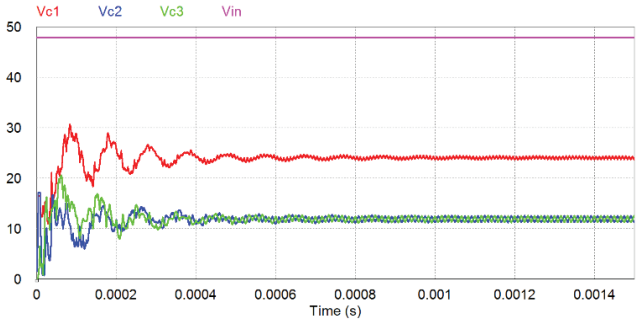

Fig. 11. Capacitor Voltage Waveforms During Start-Up Simulation, No Soft-Start

IV. Experimental Results

A. Component Selection and Loss-Breakdown

In order to properly select components for experimental results the sources of loss in the converter topology should be examined. Due to the nature of the topology the inductor value can be very small as the voltage across the inductor is only the capacitor ripple voltage. This means that the inductor loss is also hugely reduced as compared with many other converter topologies. As shown in [8] the inductor core losses are negligible, and the inductor should be optimized for a low DCR value.

The capacitor value must be selected such that the voltage ripple of the capacitor does not cause the MOSFET voltage stress to exceed the maximum rating of the device under full-load current as given by (11) where I_{max} is half of the maximum output current, $V_{DS}(max)$ is the maximum rating for the MOSFET, V_{cap} is the nominal voltage of the capacitor (either $1/2V_{in}$ for C_{f1} or $1/4V_{in}$ for C_{f2} and C_{f3}) and t_c is the charging time of the capacitor (equal to one quarter of the switching period for C_{f1} and one half of the switching period for C_{f2} and C_{f3}):

$$C > \frac{I_{max} t_c}{V_{DS(max)} - V_{cap}} \tag{11}$$

It should be noted, however, that the flying capacitors carry the load current. The efficiency of the converter is then significantly improved by minimizing the ESR of the capacitors. Therefore, in a practical design, the paralleled bank of capacitors will often be larger than the minimum capacitor value described by equation (11) in order to achieve higher efficiency. Ceramic capacitors are desirable due to their high capacitance, small size, and low ESR. The de-rating of ceramic capacitors due to the DC voltage of the capacitor, and the relatively large tolerance for the capacitance values, does not significantly influence the operation of the converter. The design does not rely on any sensitive resonant switching operation, therefore there is a high level of immunity to variation and non-idealities in components; more specifically, an increase in capacitor voltage ripple, or inductor current ripple, due to component variation would not adversely impact the operation of the converter unless the maximum ratings of the components are exceeded.

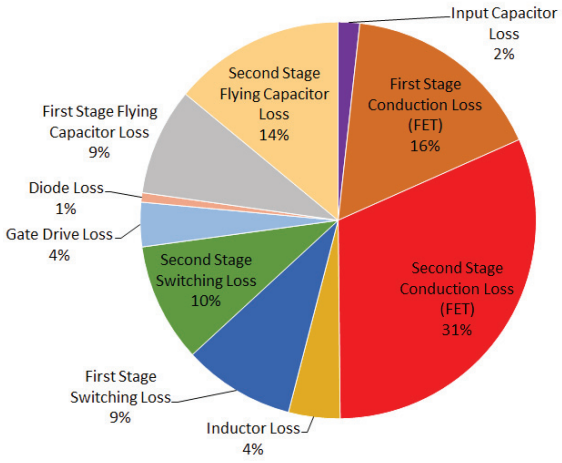

Fig. 12. 12-Switch ZIV Converter Loss Breakdown 45A Load

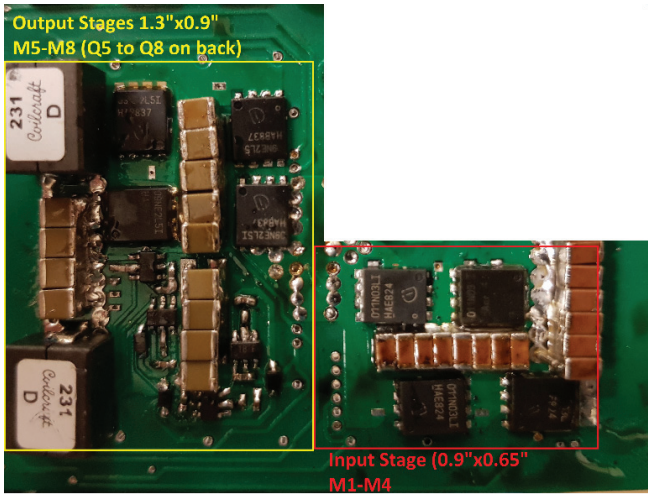

Fig. 13. 12-Switch ZIV Converter Prototype

The loss breakdown for the topology, based on the components selected in Table 3, for a full-load current of 45A, is presented in Figure 12. It should be noted that the dominant source of loss in the topology, making up over 75% of the total loss, is the conduction loss. This is because, even though the 12-Switch ZIV topology is a hard-switched topology, the switching frequency is low, and the reduced voltage stress on the individual MOSFETs significantly improves the performance of the semiconductor devices. Therefore the switching loss, and other frequency related losses, are reduced without relying on a sensitive resonant design. Additionally, the inductor losses are almost entirely eliminated, aside from the DCR loss. As the performance of semiconductor devices has continuously improved at a very rapid pace, whereas magnetics have seen only limited improvement, the ability to eliminate magnetics-related losses for the price of a higher number of semiconductor switches can offer very large improvements from both an efficiency and power density point of view.

A photo of the experimental prototype is shown in Figure 13. The components selected are outlined in Table 3. Note in Figure 13 the components outside the highlighted boxes are part of a different circuit topology not covered in this paper. The input stage occupies 0.9"x0.65", the output stages occupy 1.3"x0.9" and the overall height is 0.45".

Table 3 Prototype Components

Circuit Prototype Parameters	
C_{in}	15x4.7uF 100V X7S 1210
C_{f1}	16x10uF 50V JB 1206
C_{f2}, C_{f3}	9x47uF 25V X5R 1210
C_{out}	12x47uF 25V X5R 1210
L1, L2	230nH SLR1075-231KE
M1-M4	30V BSC011N03LSI
M5-M8, Q5-Q8	25V BSC009NE2LS5I
Switching Frequency	60kHz

B. *Normal Operation*

To verify the operation of the proposed topology the following waveforms are presented from the circuit operating at 30A load condition. Figure 14 shows the input voltage, Node 1 voltage, and output voltage for the converter. Figure 15 shows the Node 2 and Node 3 voltages, demonstrating that the proposed topology maintains the "zero inductor voltage" operation, with the inductor seeing only the capacitor ripple voltage.

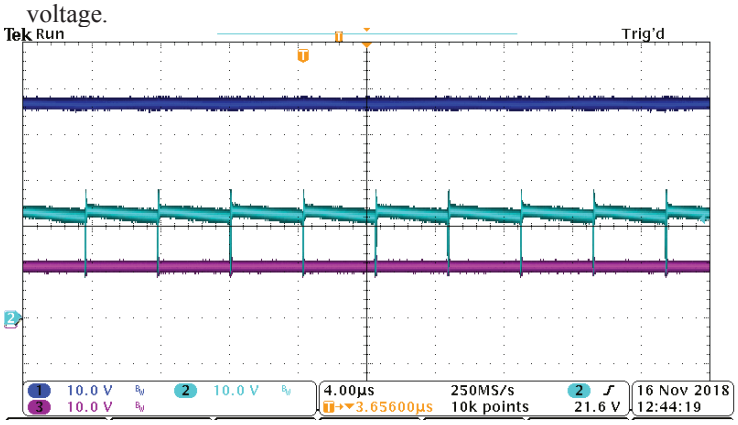

Fig. 14. Input Voltage, Node 1 Voltage, Output Voltage 30A Load

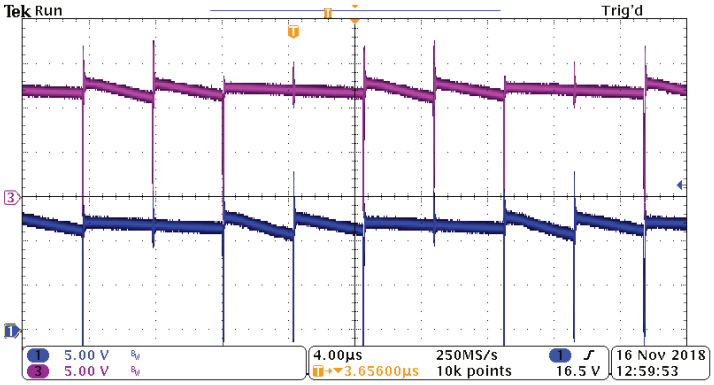

Fig. 15. Node 2 and Node 3 Voltages, 30A Load

C. Current Sharing

Figure 16 shows the AC ripple voltages for C_{f2} and C_{f3}. These ripple voltages are proportional to the capacitance value and the current carried by each phase. The two ripple voltages presented in 16 show similar values, however some variation is expected due to the tolerance of the capacitors. Therefore, in order to further verify that the current is shared evenly a thermal image of the prototype was taken.

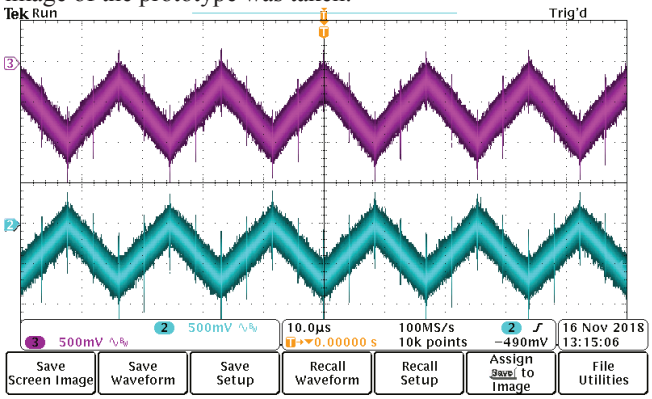

Fig. 16. C_{f2} and C_{f3} AC Ripple Voltage Waveforms, 30A Load

Figure 17 shows the thermal image of the top side of the prototype, operating at 35A load. Note in particular the temperature of M5-M8, in the lower left corner of the picture. Figure 18 shows the thermal image of the bottom side of the prototype, for Q5-Q8. For 35A load both phases show very similar thermal performance, with a difference between M5-M8 and Q5-Q8 of only around 1 degree C. It should be noted that this current sharing performance is achieved passively, through the resistive voltage drop of the circuit components. The topology provides an unregulated output voltage; therefore as current increases the output voltage will decrease a small amount proportional to the resistance of the circuit. This allows for good steady-state current sharing to be achieved without the need for active control, as demonstrated here. The large tolerance components, such as the inductor and capacitor values, do not have a large impact on the current sharing; that is to say, unlike a resonant topology, it is not critical to "match" the inductor and capacitor values, the resistance values of the components are the key enablers for passive current sharing.

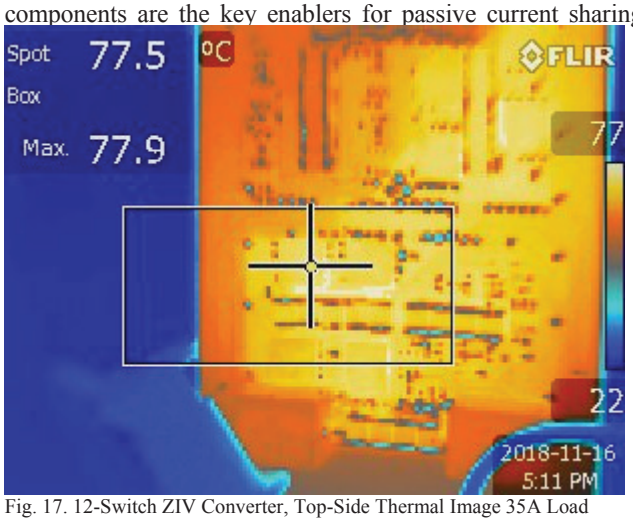

Fig. 17. 12-Switch ZIV Converter, Top-Side Thermal Image 35A Load

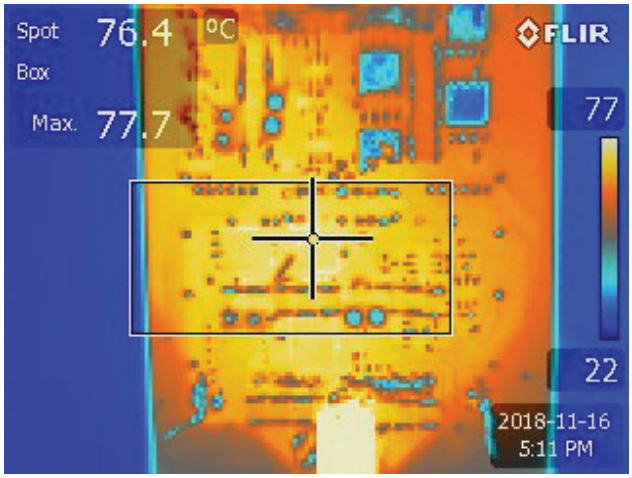

Fig. 18. 12-Switch ZIV Converter, Bottom-Side Thermal Image 35A Load

D. Efficiency Testing

The efficiency curve for the experimental prototype is presented in Figure 19. The measurements were taken using a Keithley 2700 digital multimeter, and Reidon RSN series (0.1% error) current shunts. The prototype achieves a peak efficiency of 99.2% and a full-load, 45A or 540W, efficiency of 98.5%. A thermal image of the prototype, under 45A load current, is presented in Figure 20. Notably, from the thermal image it can be seen that the loss is very evenly distributed. Additionally, the inductors at the top right, and bottom right side of the image are very cool compared with the MOSFETs and capacitors. This validates that the topology achieves very low inductor losses. 45A load current was taken to be the maximum current for the prototype, based on the converter temperature exceeding 100 degrees C for this condition. However, this is the temperature with no cooling, and no heatsink. In order to achieve higher output current, a second test was conducted using a small USB-powered desk fan, pictured in Figure 21, to achieve higher output current.

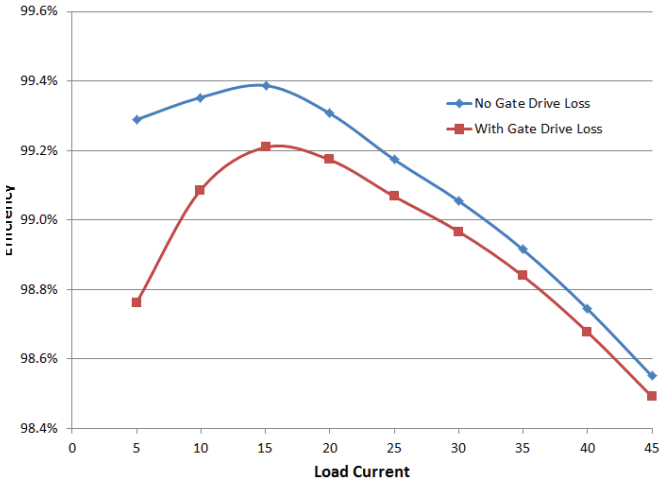

Fig. 19. 12-Switch ZIV Converter Efficiency Curve, No Cooling

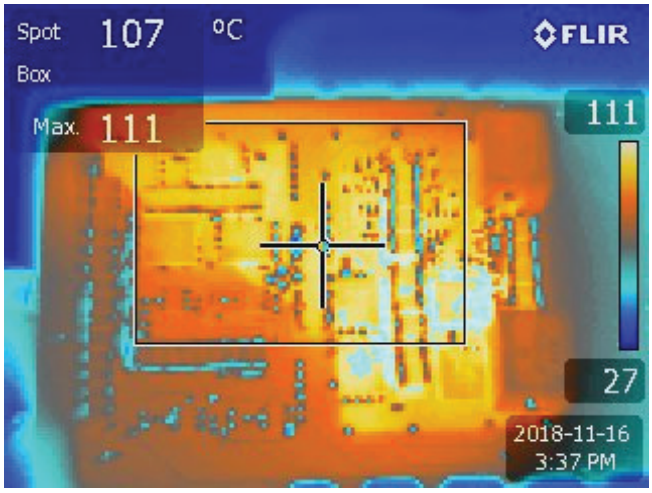

Fig. 20. 12-Switch ZIV Converter, Thermal Image 45A Load, No Cooling

Fig. 21. USB Desk-Fan

The efficiency curve for the fan testing, as compared with no fan, is presented in Figure 22. For both curves the gate-drive loss is included in the efficiency measurement.

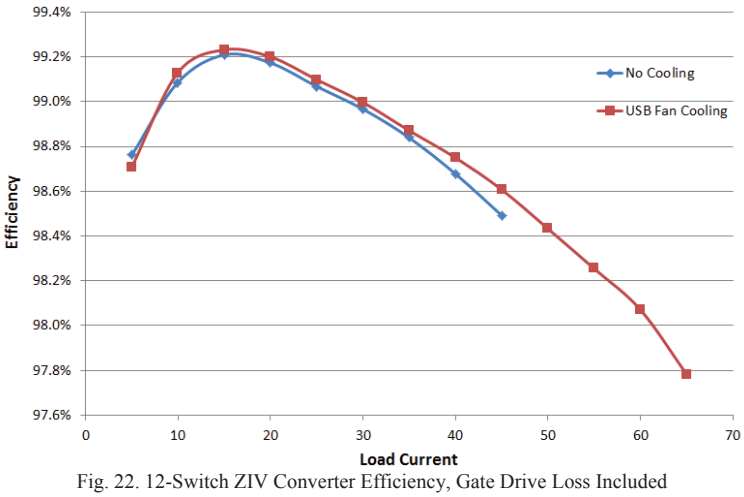

Fig. 22. 12-Switch ZIV Converter Efficiency, Gate Drive Loss Included

The performance with the fan is very similar at light load, however, at higher load the efficiency is improved. This is due to a reduction in the temperature rise of the MOSFETs. The on-resistance of the MOSFETs can increase by up to 50%, compared with the on-resistance at room temperature, when the device temperature exceeds 100 degrees. Therefore, operating a fan improves the efficiency of the prototype when these thermal effects start to have significant impact, while also allowing for much higher load current to be achieved. The maximum load current using the USB fan cooling is 65A. A thermal image of the prototype operating at this condition is presented in Figure 23.

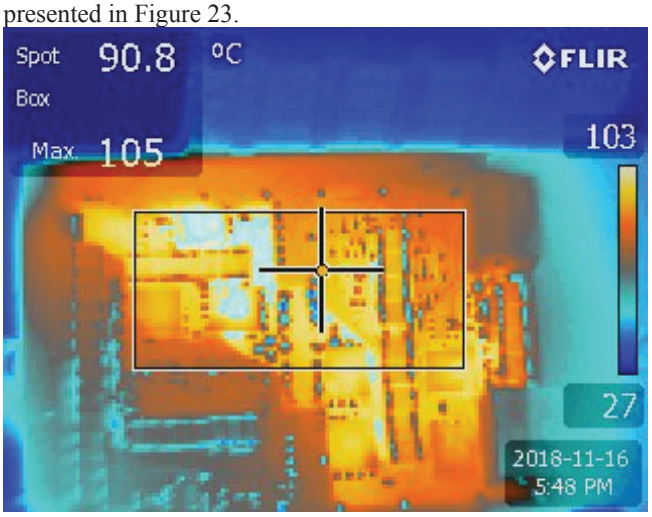

Fig. 23. 12-Switch ZIV Converter, Thermal Image 65A Load, Fan Cooling

V. Discussion on Switched Capacitor Converters

The ZIV converter topology relies on utilizing low voltage rated MOSFETs, and minimizing reliance on magnetic components to achieve high efficiency. This similar design philosophy has led to a resurgence in switched capacitor converter topologies in recent years, with some works targeted specifically at the 4:1 conversion ratio bus converter such as [11] and [12].

A fundamental problem with true switched capacitor converters is known as the charge redistribution loss mechanism [19]. When a low impedance switch connects two capacitors that are at different voltage levels (such as due to capacitor voltage ripple) there will be a current inrush, and energy loss associated with charge redistribution. This leads to higher RMS current stress for the switches. The energy loss can be reduced by increasing the switching frequency, or the size of the capacitors, but in both cases this results in a loss of efficiency or power density.

To overcome the problems associated with this charge redistribution loss, many switched capacitor converter topologies use an added inductor to allow for lossless switching. As discussed in [10] many of these switched-capacitor topologies that utilize an additional inductor are highly sensitive to component variations; requiring resonant operation or precisely determined capacitor values [14]-[18] or

additional sensing of the capacitor voltages [13] to achieve soft-charging. By contrast, the ZIV converter topology does not rely on any precisely tuned component values and requires no additional sensing circuitry; the capacitors should be sized appropriately to ensure that the MOSFETs do not exceed their maximum voltage rating, but this can be achieved with significant margin when considering that it is desirable to use larger capacitors to minimize the size of the inductor by reducing capacitor voltage ripple, and also to reduce the ESR of the capacitor banks.

It is also a challenge to parallel multiple phases when using resonant converters, as the operation of these converters will change based on component variations. Scaling complex control circuitry to a large number of phases can also present a challenge.

As demonstrated in this paper the ZIV converter topology can achieve good current sharing with off-the-shelf components that have an inherently wide variation, and no active control. The ZIV topology is able to operate at fixed frequency, and fixed duty cycle, to achieve 4:1 stepdown with no control required to maintain current sharing or balance the capacitors.

VI. Conclusions

As compared with the standard ZIV converter the proposed topology offers significant improvements. The key driving factor behind this improvement is the superior utilization of the first stage switches. This allows for a significant reduction in the RMS current carried by these MOSFETs and the flying capacitor, and additionally, the increase to 50% duty cycle significantly reduces the input capacitor ESR losses.

Compared with a true two-phase ZIV converter, the proposed topology uses 2 fewer switches (12 compared with 14) as well as allowing for the elimination of one flying capacitor which, as discussed in section IV-A, must be relatively large to minimize the ESR and ensure the capacitance value is high enough to maintain safe operation for the MOSFETs. The penalty for this size reduction, compared with a two-phase ZIV converter, is the two additional MOSFETs M5 and Q5 in the output stages which result in slightly increased losses.

The steady-state current sharing of the topology is verified by examining both the flying capacitor ripples of the output stages, as well as a thermal image of the MOSFETs. This current sharing is achieved passively.

With no fan cooling the converter achieves a maximum of 540W output, with a full load efficiency of 98.5% and a peak efficiency of 99.2%. With the addition of USB desk fan for cooling the maximum output of the prototype was raised to 780W, with a full load efficiency of 97.8%.

The input stages occupies an area of 0.9”x0.65”. The two output stages occupy an area of 1.3”x0.9”. The inductor height is 0.3”, the tallest capacitor is 0.1”, and the board thickness is 0.05”. The power density of the prototype is 990W/in^3 as measured by the smallest box volume the converter could occupy. It should be noted that the inductor is by far the tallest component of the board, with a height of 0.3 inches compared with maximum of 0.1 inch height for the other components. This off-the-shelf inductor could be replaced by a thinner package to further improve the power density of the converter.

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